Area-Power-Efficient 11-Bit SAR ADC with Delay-Line Enhanced Tuning for Neural Sensing Applications

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Abstract—In this paper, an area-power-efficient 11-bit hybrid analog-to-digital converter (ADC) with delay-line enhanced tuning for neural sensing applications is presented. To reduce the total amount of capacitance, this hybrid ADC is composed of a coarse tune and a fine tune by 3-bit delay-lined-based ADC and 8-bit successive approximation register (SAR) ADC, respectively. The delay-lined-based ADC is designed to detect the three most significant bits by a modified vernier structure. To relax the accuracy requirement of the coarse tune, the lifting-based searching algorithm and re-comparison procedure are proposed for the fine tune. To further achieve energy saving, split capacitor array and self-timed control are utilized in the SAR ADC. Fabricated in TSMC 0.18 μm CMOS technology, an ENOB of 10.4-bit at 8KS/s can be achieved with only 0.6μW power consumption and 0.032-mm² area. The FoM of this ADC is 49.4fJ/conversion-step.

I. INTRODUCTION

Highly integrated neural sensing microsystems for capturing accurate signals are crucial for brain function investigation and neural prostheses realization [1]. In neural sensing microsystems, recording amplifiers and analog-to-digital converters (ADCs) are essential to record and transfer physiological signals into digital signals for further signal processing. Among several types of ADCs, successive approximation register (SAR) ADCs are broadly adopted for bio-signal sensing applications due to moderate resolution accuracy, medium speed and low power consumption [2-4].

A conventional SAR ADC usually consists of a comparator, control logic and a digital-to-analog converter (DAC) implemented by a capacitor array. However, the total amount of capacitors increases exponentially with the increasing resolution of a SAR ADC, causing dramatic increases of area and power consumption. Therefore, minimizing the size of capacitor array has become one of the critical design challenges in SAR ADCs, especially for high resolution SAR ADCs. In this work, an 11-bit hybrid ADC with Delay-Line Enhanced Tuning is proposed. This hybrid ADC is composed of a 3-bit delay-line-based ADC and an 8-bit SAR ADC for coarse-tuning and fine-tuning, respectively. The delay-line-based ADC can effectively reduce the total capacitance in the SAR ADC.

II. 11-BIT HYBRID ADC

The hybrid ADC consists of a 3-bit delay-line-based ADC and an 8-bit SAR ADC as shown in Fig. 1. The 8-bit SAR ADC is designed as a fine tune block to provide moderate resolution accuracy and low energy consumption. Additionally, the delay-line-based ADC is designed as a coarse tune block to enhance tuning and reduce the total capacitance of the SAR ADC. The details of the coarse tune and fine tune are described as follows.

A. Delay-Line-Based Enhanced Tuning Block

The delay-line-based enhanced tuning block is a combination of a voltage-to-time converter (VTC) and a time-to-digital converter (TDC). Based on P-type and N-type voltage controlled delay cells [5], the time differences of different voltages can be derived, and hence the input voltage can be divided into 8 groups with 3-bit detection. The conventional TDC consists of a set of buffers and flip-flops. Moreover, the vernier structure of TDC can reduce the delay difference of each stage of buffer to \( \delta \) [5]. If the quantizing voltage of \( V_{in} \) is between \( V_a \) and \( V_b \) with an R-bits resolution, the total processing time window, \( T(V_{in}) \), is between \( T_a \) and \( T_b \). Assume \( T(V_{in}) \) is a linear function of \( V_{in} \), then

\[
T_b - T_a = \delta \cdot 2^R \quad (1)
\]

However, maintaining the linearity of the time window from \( V_a \) to \( V_b \) is a design bottleneck for delay-line-based ADCs. Therefore, a modified vernier structure of the TDC is proposed for the delay-line-based enhanced tuning block as shown in Fig. 2. Instead of designing a linear VTC, the delay between two buffers in the modified TDC is adjusted from \( \delta \)
The basic concept of voltage detection in a SAR ADC is to charge the capacitor INP to the correct value in Eq. (3) and Eq. (4) and the voltage of INN is changed to \( V_{DD} - V_{IN} \) or \( V_{IN} \), which is connected to ground. Hence, \( V_{INP} \) could be positive to \( V_{IN} \) and \( V_{INN} \) has the probability of being below the threshold voltage \( V_{TH} \). Therefore, the time difference of the two buffers in each stage is adjusted for the corresponding input voltage as shown in Eq. (2).

\[
T_b - T_a = \sum_{n=1}^{8} \delta_n
\]  

(2)

The proposed structure can provide better precision compared to the original vernier structure.

**B. Design of 8-Bit SAR ADC**

The basic concept of voltage detection in a SAR ADC is to compare \( V_{IN} \) with a reference voltage (e.g. ground). The SAR control logic adjusts the voltage level related to \( V_{IN} \) by turning on or off the switches of the capacitor array. As shown in Fig. 3(a), the capacitor \( C_{INP} \) is charged with the voltage \( V_{IN} \). Accordingly, by switching the bottom nodes of these capacitors connected to \( V_{DD} \) or ground, the range of \( V_{IN} \) is from \(-V_{TH}\) to \( V_{DD} - V_{IN} \) (or \(-V_{TH} + \Delta V\) to \( V_{DD} \)). The comparator is designed to compare \( V_{INP} \) and \( V_{INN} \) which is connected to ground. Hence, \( V_{INP} \) could be positive or negative and \( V_{INN} \) (ground) by adjusting \( \Delta V \) bit by bit. However, this basic operation of SAR ADCs is not adopted in our SAR ADC. Based on the comparator proposed in [6] with single-ended input, both inputs of the comparator may be too low to turn on the input NMOSs. Therefore, a symmetric adjusting comparison method is utilized as shown in Fig. 4(b). Instead of comparing GND and \(-V_{IN}\), the starting voltages of INP and INN are changed to \( V_{DD} - V_{IN} \) or \( V_{IN} \) based on the condition as the following.

\[
V_{INP} = \text{Maximum} \left( V_{DD} - V_{in}, V_{in} \right) + \Delta V1
\]  

(3)

\[
V_{INN} = \text{Minimum} \left( V_{DD} - V_{in}, V_{in} \right) + \Delta V2
\]  

(4)

Where \( \Delta V1 \) and \( \Delta V2 \) are adjustable voltages controlled by the switched capacitors of INP and INN. Therefore, the initial voltages of \( V_{INP} \) and \( V_{INN} \) are between \( V_{DD} \) to \( V_{DD}/2 \) and \( V_{DD}/2 \) to ground, respectively. The capacitor array of INP and INN can be charged to the correct value in Eq. (3) and Eq. (4) by the first bit of coarse-tune ADC. As such, only \( V_{INP} \) or \( V_{INN} \) has the probability of being below the threshold voltage of NMOSs, thus guaranteeing the functionality of the comparator. Moreover, the difference of \( V_{INP} \) and \( V_{INN} \) becomes \( 2 \cdot V_{IN} \) instead of \( V_{IN} \) to increase the precision of the SAR ADC. The voltage difference between \( V_{INP} \) and \( V_{INN} \) is as shown in Eq. (5).

\[
V_{INP} - V_{INN} = \left| V_{DD} - 2 \cdot V_{in} \right| + (\Delta V1 - \Delta V2)
\]  

(5)

In the hybrid ADC, the coarse-tune ADC propagates the three most significant bits (MSBs) to the SAR control logic. Based on these three bits, a lifting-based searching algorithm is proposed for the SAR ADC to relax the accuracy requirement of the coarse tune. After sampling the input voltage, a lifting procedure lifts \( V_{INN} \) up to the level slightly higher than \( V_{INP} \) as shown in Fig. 4. The whole operation region is divided into 8 blocks, and the lifting procedure lifts \( V_{INN} \) one block higher than that of \( V_{INP} \). After lifting, the capacitor array of INP operates as a conventional DAC of the SAR ADC as shown in Fig. 5. However, the starting bit in the SAR ADC is the 4th bit of \( V_{IN} \), so the reference voltage for the capacitor array of INP should be shrunk. Accordingly, the
difference between two inputs of the comparator is 2V_{DC}, and the reference voltage of INP is V_{DD}/4.

C. Re-comparison Procedure

In the hybrid ADC, three clock cycles are required for a sample as shown in Fig. 6. The first clock cycle is for the coarse-tune to detect the 3 MSBs, and the second clock cycle is for the fine tune. In this cycle, the sample stage and the comparison stage of the SAR ADC operate when the clock are “High” and “Low”, respectively. However, a 30mV offset of the 8 detection blocks in the coarse-tune ADC is designed to prevent the uncertain process-voltage-temperature (PVT) variations on the delay cells. Based on the offset detection region, the 3MSBs may indicate the wrong block for the fine tune. Therefore, V_{INN} would be lifted too high, and thus produces a totally wrong output (i.e. output = 1111'1111). Since the offset is inevitable, a re-comparison procedure should be inserted in the third clock cycle.

As soon as a comparison of the SAR ADC has been done, a verification process would examine whether the output is “1111’1111” or not. Once the straight-one output is detected, the fine-tune ADC would start over again in the third clock cycle with 3MSBs+1. The re-comparison procedure can relax the accuracy requirement of the coarse tune with acceptable overhead on power consumption and performance.

III. CIRCUIT DESIGN OF SAR ADC

To further reduce the total capacitance of the capacitor array, the technique of split-capacitors [7, 8] is utilized in the SAR ADC. With a 1C bridge capacitor, the total capacitance for INP is shrunk from 128C to only 32C. To balance the capacitance of INP and INN, the total capacitance of INN is shrunk to the same scale. Therefore, the area and power consumption of the capacitor array decrease significantly. Fig. 5 also presents the architecture of SAR ADC with split-capacitor array.

Because the split-capacitor array would be severely affected by noises, switches are added between INP, INN and the comparator to isolate the parasitic capacitance of the comparator. A switch between two inputs of the comparator is also inserted to reset the comparator at the beginning of comparison. Other switches are placed between input nodes and the capacitor array as two-stage switches to reduce the parasitic capacitances.

To reduce power consumption, a two-stage low leakage dynamic comparator is utilized [6]. The first and second stages are an amplifier and a generative latch, respectively. However, this comparator has a serious weakness for the single-ended sensing. As both inputs of the comparator are smaller than the threshold voltage of NMOS, the amplifier cannot provide enough current to trigger the latch. Thus, the latch requires much longer time than usual to produce the results. Therefore, the symmetric adjusting comparison is proposed to effectively prevent this problem caused by low-voltage input of both sides.

For the SAR ADC architecture, self-timed SAR control can provide the advantages of slow operation clock, fast sampling rate and high power efficiency. First, for self-timed circuit, once comparator completes the comparison of one bit, the comparison of the next bit can start without any delay, and the period of each comparison is not fixed but dynamically adjusted according to the corresponding delay. Another advantage is that the system clock is no longer required to control the comparator, and thus the frequency of the system clock can be lowered. The system clock is reduced from 333MHz to lower than 1MHz while maintaining the same sampling rate. Thus, a significant improvement of the overall system power consumption can be achieved.

The proposed self-timed SAR control is implemented by Muller C-elements as shown in Fig. 7. The output of Muller C-element would transmit the value of inputs only when both inputs match. In other cases, the output maintains its original value until two inputs become the same again. With the cascaded Muller C-element structure, a simple but efficient signal transmission circuit is available for the self-timed control. At the beginning, all outputs of Muller C-element are reset to “1”. As “Comparator_Done” switches from “1” to “0” or from “0” to “1”, the transmission of “0” would pass through one Muller C-element. After 16 iterations, the value of the cell which named “Prev.Done [7]” would be pulled down, and terminates the comparison. Therefore, the eight-bit comparison can be realized without any external timing control signals.

IV. EXPERIMENT RESULTS

The prototype of the hybrid ADC has been fabricated in TSMC 1P6M 0.18μm CMOS process. The chip microphotograph of the proposed ADC is shown in Fig. 8, and the active area of the ADC is 0.032mm$^2$ (252μm x 126μm). The total capacitance of DAC for SAR ADC is 7.45pF and the unit capacitance is 0.15 pF. In the coarse tune, the capacitance of the two capacitors for the N-buffer and P-Buffer is only 80fF. The area of the coarse tune is 30μm x 126μm. Based on the design of the delay-line enhanced tuning, the size of the DAC in the SAR ADC can be reduced significantly. Compared with the conventional 11-bit SAR ADC, the area is reduced by 42% in the proposed hybrid ADC under the same resolution.
The total power consumption of the hybrid ADC is 0.6 μW at 8KS/s. The maximum sampling rate of this ADC is 1.2MS/s. Fig. 9 presents the FFT spectrum with 8 Ks/s sampling frequency and 180 Hz input frequency. The DNL and INL are as shown in Fig. 10. The DNL is +0.7/-1.0 LSB and the INL is +0.8/-0.9 LSB. Table I compares the proposed SAR ADC with delay-line enhanced tuning and other SAR ADCs under similar sampling rates and resolutions. To compare the effective area of different SAR ADCs, a normalization factor considering the FoM and area is applied. This normalization factor is the product of the FoM and the active area divided by 2R to normalize the effect of different resolutions, where R represents the resolution of an ADC. Compared with other ADCs, the proposed hybrid ADC achieves the most power-area efficiency.

V. CONCLUSION

In this paper, an 11-bit SAR ADC with delay-line enhanced tuning for neural sensing is presented for improved power and area efficiency. This hybrid ADC composes of a course tune stage and a fine tune stage. By reducing the total amount of capacitance, the hybrid ADC reduces the area by 42%. An ENOB of 10.4-bit at 8KS/s is achieved with only 0.6μW power consumption. Therefore, this hybrid ADC is suitable in bio-medical sensing systems.

REFERENCES


