Low Temperature Bonding of Sn/In-Cu Interconnects for Three-Dimensional Integration Applications

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ABSTRACT

A low temperature bonding technology of Sn/In composite solder bonded to Cu interconnect is proposed and investigated. The intermetallic compounds formed in the bonded interconnects can survive well in the following process. The Sn/In-Cu interconnects bonded at low temperature all exhibit excellent electrical performance and high resistance to multiple current stressing, showing a great potential in 3D applications.

INTRODUCTION

Bonding technology, including chip-to-chip, chip-to-wafer, and wafer-to-wafer bonding, is a key fabrication process in 3-D integration. Cu-Cu thermo-compression bonding has become the attractive candidate for interconnect bonding since Cu has excellent electrical properties and is preferred material in semiconductor metal level. However, high bonding temperature above 300 °C for Cu-Cu bonding is necessary to achieve the excellent bonding quality, which might lead to thermal stress issue and bonding misalignment. High temperature bonding could also degrade the performance of devices. Consequently, a low temperature bonding is essential to fulfill the requirement of low thermal budget and has better process compatibility in heterogeneous integration applications.

Eutectic bonding is a potential candidate for the low temperature bonding, and provides a great tolerance of surface morphology, particle contaminants, and vacuum requirement. In/Sn based low temperature bonding is a promising candidate since the eutectic melting point of In-48 at. % Sn alloy is only 118°C. Previous studies for In/Sn based bonding were focused on MEMs hermetic bonding investigation or bulky solder research without electrical properties and reliability investigations [2-5]. In addition, a complete consumption of In and Sn atoms in the bonded interlayer is required due to the requirement of following high processing temperature, which is usually higher than the melting point of In (156.6 °C) and Sn (231.9 °C).

In this work, we report the study Sn/In-Cu bonding, both in chip-to-chip level and wafer-to-wafer level. Bonding at different low temperatures was performed respectively and the bonding quality was investigated by SAT analysis, TEM/EDX, and Grazing Incident Diffraction analysis. Contact resistances and current stressing results were also showed in this research. In and Sn atoms are apparently dissolved into Cu interconnect, and the Cu-In-Sn IMCs formed in our approach represented a continuous solid solution between the Cu-Sn and Cu-In systems with a high melting point of 500 °C [5].

EXPERIMENT

The Sn/In-Cu bonding structure for this research is schematically shown in Fig. 1. SiO₂ was formed on silicon wafer by TEOS with a thickness of 300 Å. A thin layer of Pt with a thickness of 300 Å was deposited on Si/SiO₂ substrate using E-beam evaporation. Two layers of Sn/In solder with a thickness of 2600 Å and 2600 Å were deposited sequentially using thermal coater in one vacuum cycle. The atomic percentages of Sn in this In-Sn solder alloy layers were nearly 50%, which means that when the bonding temperature was increased over 118 °C of the In-Sn eutectic point, In-Sn eutectic liquid phase could formed and would dissolve the remaining solid Sn and In [6]. To demonstrate the bonding scheme, layers of Ti/Cu with thickness of 200 Å and 3000 Å were sequentially sputtered on another Si/SiO₂ substrate. Here the Pt and Ti layers were acted as an adhesive layer. Before bonding, Cu surface was cleaned by acetic acid to remove copper oxidation [7]. The bonding pairs were then bonded face to face for 50 min at 180 °C, 160 °C, and 140 °C, respectively. The composition and microstructure of the bonded structures were analyzed by TEM, EDX, and Grazing Incident Diffraction analysis.

The contact resistances of Sn/In-Cu low temperature bonding were evaluated by Kelvin structure of the bonding area, with the size of 25 μm × 25 μm. The current stressing cycling test was evaluated for 1000 cycles of sweeping current from -100 mA to 100 mA.
A. Evaluation of Sn/In-Cu Bonded Interconnects

The quality of wafer level bonded sample at 180°C was evaluated by scanning acoustic tomography (SAT), as shown in Fig. 2. The SAT image shows a well-bonded result across the wafer. The XRD analysis on bonded interconnects shows that $\eta$-Cu$_6$Sn$_5$ was found in the sample bonded at 180 °C without Sn or In peaks, as shown in Fig. 3. The XRD results suggest that In and Sn atoms were completely consumed and reacted with Cu after bonding.

TEM analysis of the bonded sample in Fig. 4(a) shows a uniform bonding interface without voids. In Fig. 4(b), EDX line scan analysis in the bonded structure shows the composition profile of approximately 60 % Cu, 20 % Sn, and 20 % In. According to the Cu-In-Sn system interface reaction research reported by Sommadossi et al. [4], the IMC formed in the bonding reaction zone should be $\eta$-Cu$_6$(Sn,In)$_5$. Electron diffraction analyses were performed to identify the crystal structure of Cu$_6$(Sn,In)$_5$. The cross-section of Sn/In-Cu bonded interface from 180 °C bonding is presented in Fig. 5(a), where the diffraction patterns are indicated in Fig. 5(b) and (c). The results show that during bonding In and Sn atoms diffused into Cu layer of another wafer to form poly-Cu$_6$(Sn,In)$_5$, while the Cu atoms diffused into Sn/In alloy layer to form single crystal Cu$_6$(Sn,In)$_5$.

Due to the Sn-In binary system with an eutectic temperature of 118 °C, In atoms would interdiffuse with Sn atoms to form a thin liquid solution at the interface between In layer and Sn layer at 118 °C [6]. As the bonding temperature reached 180 °C, the liquid phase dissolved the adjacent In and Sn atoms and the molten solder layer eventually diffused into Cu pad to form poly crystal Cu$_6$(Sn,In)$_5$ phase. However, the Cu atoms also diffused into molten solder to form single crystal Cu$_6$(Sn,In)$_5$. Due to the melting point of Cu$_6$(Sn,In)$_5$ is about 500 °C, the Sn/In-Cu interconnects bonded at low temperature allowed application at high service temperatures in a low thermal budget procedure. This result agreed with the phase identification suggested by the EDX line scan and XRD analysis.
B. Contact Resistance Measurement

The contact resistances of Sn/In-Cu interconnects bonded at 180 °C, 160 °C, and 140 °C, respectively, are shown in Fig. 6. The specific contact resistance $\rho_c$ was approximately $1.25 \times 10^{-5}$ Ω·cm$^2$ both at 180 °C and 160 °C, while approximately $5 \times 10^{-5}$ Ω·cm$^2$ at 140 °C. There was no deviation of resistance during measurement, indicating a reliable bonded structure with a stable electrical performance was formed during the low temperature bonding procedure.

C. Multiple Current Stressing

To evaluate the stability of Sn/In-Cu bonded interconnects, the contact resistances of interconnects bonded at 180 °C, 160 °C, and 140 °C were investigated after 1000 current stressing loops, as shown in Fig. 7. Both the contact resistances bonded at 180 °C and 160 °C are approximately 0.02 Ω, while that bonded 140 °C is approximately 0.08 Ω. This result suggests that the Sn/In-Cu bonded interconnect was reliable and could withstand a long term electrical current.

CONCLUSION

Sn/In-Cu interconnects bonded at low temperature have been developed and evaluated for 3-D integration. The full presence of Cu$_6$(Sn,In)$_5$ with a melting point of 500 °C formed in this interconnect meets the requirement of following high processing temperature. The bonding performed at 140 °C, below the melting points of Sn and In, exhibits similar great electrical properties and reliability against current stressing to the interconnects bonded at 160 °C and 180 °C. The Sn/In-Cu bonding technology has the great potential in low thermal budget 3-D integration applications.

REFERENCES