Wireless Neural-Sensing Microsystem using TSV-Embedded Dissolvable μ-Needle Array and Flexible Interposer

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Abstract—For implanted neural-sensing devices, one of the remaining challenges is to transmit stable power/data (P/D) transmission for high spatiotemporal resolution neural data. This paper presents a miniaturized implantable 128-channel wireless neural-sensing microsystem using TSV-embedded dissolvable μ-needle array, a flexible interposer and 4 dies by 2.5D/3D TSV heterogeneous SiP technology. The 4 dies are 2 neural-signal acquisition ICs implemented by 90nm CMOS, 1 neural-signal processor by 40nm CMOS and 1 wireless P/D transmission circuitry by 0.18μm CMOS. Thus, the proposed wireless microsystem realizes 128-channel neural-signal sensing within the area of 5mm x 5mm, neural feature extraction and wireless P/D transmission using an on-interposer inductor. The overall average power of the circuits in this microsystem is only 9.85mW.

I. INTRODUCTION

Ultra-high-density neural-sensing microsystems enable monitoring and mapping of brain activities by capturing high spatiotemporal resolution neural data [1]. To obtain high-resolution neural signals, neural implant microsystems should meet some critical constraints such as small form factor, ease of implantation and longevity. Several highly miniaturized neural-sensing microsystems have been presented for acquiring local field potentials (LFPs) or electrocorticogram (ECoG) [2-4]. These microsystems typically compose of three main parts 1) invasive probes/electrodes for biopotential collection, 2) low-power circuits for brain signal feature acquisition, extraction, classification and transmission, 3) low-noise electrical link wires between electrodes and circuits for signal integrity. In these approaches, however, the sensing density for high spatiotemporal resolution is limited by the shape, pitches and impedance of the probes and the routing density of link wires.

For obtaining high spatiotemporal resolution neural data, feature extraction and classification is an essential function to reduce the required bandwidth of wireless data transmission. In view of this, the overall power consumption is also reduced with the decreasing data rate. In this paper, a miniaturized implantable 128-channel (128-CH) wireless neural-sensing microsystem is proposed using TSV-embedded dissolvable μ-needle array, a flexible interposer and 4 dies as shown in Fig. 1. The 4 dies are designed for high-density neural-signal acquisition, feature extraction and wireless power/data (P/D) transmission. The 2 64-CH neural-signal acquisition dies are designed to sense high-density 128-CH ECoG signals via 128 low-noise neural amplifiers and 32 area-power-efficient analog-to-digital converters (ADCs) [5]. Additionally, feature extraction and classification is realized via a neural-signal processor using 40nm CMOS technology. This neural processor is implemented by ARM Cortex-M0 and low-power discrete wavelet transform (DWT) accelerators. For transmitting the ECoG features, wireless P/D transmission circuitry is designed to transfer data through an on-interposer inductor.

II. HETEROGENEOUSLY INTEGRATED WIRELESS NEURAL-SENSING MICROSYSTEM

The high-density wireless neural-sensing microsystem is realized and integrated by 2.5D/3D TSV heterogeneous system-in-package (SiP) technology. The TSV-embedded μ-needle array and 4 dies are integrated on the biocompatible Cu-Via flexible interposer using chip-to-chip ENIG bonding and 2.5D/3D TSV integration technologies as shown in Fig. 2. The SiP technology provides heterogeneous integration, high-density routing capability and short link wires for the high-resolution neural-sensing microsystem. The electrical characteristics of the TSV-embedded μ-needle array and Cu-Via flexible interposer have been introduced in [6].

The 4 dies are designed for high-density neural-signal acquisition, feature extraction and wireless power/data (P/D) transmission. Fig. 3 presents the system block diagrams of the heterogeneous 128-CH wireless neural-sensing microsystem.
composited of two 64-CH neural-signal acquisition dies (die-3 & die-4, 90nm), 1 neural-signal processor (die-1, 40nm) and 1 wireless P/D transmission circuitry (die-2, 0.18μm). These 4 dies are partitioned and implemented with different process nodes based on the power/area/cost trade-off. Additionally, the die sizes of die-1, die-3 and die-4 are all 3mm x 3mm set by the minimal size of ENIG bonding, and the size of die-2 is 1.2mm x 1.2mm by C4 flip-chip bonding since its I/O pin number is much less than those of other dies. Each 64-CH neural-signal acquisition circuitry is composed of 16 4-CH low-noise chopper-stabilized neural amplifiers and 16 area-power-efficient hybrid ADCs. The detail of the 64-CH neural-signal acquisition circuitry has been presented in [6], and the overall power of these two dies is only 1.9mW. The neural-signal processor is designed to control this microsystem and to extract and classify features for reducing the required bandwidth of data transmission. For battery-less biomedical implants, power and data telemetry are realized and transmitted through an on-interposer inductor. The detail of the neural-signal processor and P/D transmission circuits are described in the following sections.

III. NEURAL-SIGNAL PROCESSOR WITH ONE-TIME PROGRAMMING MEMORY

The neural-signal processor adopts ARM Cortex-M0 to manage the data flow and cluster the data for medical diagnosis by filtering the features into different frequency bands. The boot code of this processor is stored in a 320kB on-chip one-time programming (OTP) memory. Fig. 4 presents the control and datapath of the boot OTP memory in the neural-signal processor. Before implanting this microsystem in a brain, the boot code is programmed to the OTP memory via a 12-pin connector. After programming, this connector would be removed and the OTP memory is changed to the execution mode for reading instructions by welding to the ground on the interposer. In the execution mode, the reset signal initializes the implanted microsystem by a self-reset circuitry as shown in Fig. 5. An integrated voltage regulation module (VRM) in the OTP memory generates a ready signal (at the end of the critical path in the wireless power deliver network) when the boosted voltage reaches the operation voltage. To enhance the timing tolerance to the total settling time of the power network, the reset signal is generated behind the ready signal by around 41μs using a positive edge-detector and a 12-bit counter to increase the safety timing margin.

Fig. 3. Block diagrams of the heterogeneous 128-CH wireless neural-sensing microsystem

Fig. 4. Control and datapath of the boot OTP memory.

Fig. 5. Self-reset circuitry for wireless neural-sensing circuitry.

Fig. 6. Architecture of a 16-CH configurable DWT PE.
In addition to increase the energy-efficiency of the neural-signal processor, 8 16-CH configurable discrete wavelet transform (DWT) processing elements (PEs) are realized to accelerate the high-resolution feature extraction. The power consumption of each DWT PE would increase rapidly when the number of channel is larger than 16 due to the complex wire routing. Fig. 6 shows the datapath of 1 configurable DWT PE which is implemented by a lifting-based DWT algorithm [2]. The timing windows, channel numbers, frequency bands and mother wavelets can all be adjusted by setting the configuration status register.

### IV. HIERARCHICAL WIRELESS POWER MANAGEMENT UNIT

The wireless P/D transmission circuitry receives wireless power by the inductive coupling via an on-interposer inductor, and regulates power to different voltage levels and loading conditions for other circuits through a full-bridge rectifier and a high-efficiency hierarchical power management unit (PMU). As both the power and data transmission share the same coupling channel with different directions, the power and data are transmitted alternately based on an interleaved time-tracking technique as shown in Fig. 7. The power source is only transferred during half cycle, and the two non-overlapped signals, $\Phi_1$ and $\Phi_2$, are generated by the power detector and the valid signal of transmitted data. These two signals assign the permission of the inductive coupling channel to the power regulation or data transmission circuits.

The topology of this wireless hierarchical PMU is designed by cascading three-level step-down voltage regulation after the optimization of the overall power efficiency as shown in Fig. 8. The design criterion of the PMU is to provide stable and fixed voltages. Thus, the hierarchical PMU is realized by 1 bandgap voltage reference, 2 switched capacitor (SC) DC/DC converters and 2 low-dropout (LDO) regulators. These two SC DC-DC converters are utilized to convert the same voltage ratio from 3.0V to 1.5V and 1.2V to 0.6V, respectively. The characteristics of the hierarchical PMU are listed in Table I, and the overall power efficiency is 68.4%. To provide stable voltages, off-chip capacitors are utilized and mounted on the interposer.

### V. LOW-POWER WIRELESS DATA TRANSMISSION

For the wireless data transmission, on-off keying (OOK) modulation is utilized for the short-distance wireless communications as shown in Fig. 9. For reducing the power consumption, a free-running voltage-controlled oscillator (VCO) is adopted to generate the carrier signals for the non-coherent OOK modulation. The VCO is realized by current-starved ring-inverters with a bandgap voltage reference. The current-starved circuits as shown in Fig. 10 and bandgap voltage reference provide stable current and control voltage to oscillate at a fixed frequency against PVT variations. Thus, the frequency range of the VCO is within 388MHz to 416MHz for...
the target 400MHz as shown in Fig. 11, and the S-parameters (S12 and S21) of the inductive coupling is also measured when the distance is 0.5cm. The insertion loss is above -10dB when the frequency is within 365MHz to 430MHz. As the maximum required data bandwidth is 3.2Mb/s without filtering any features, the data rate for the OOK modulation is 8Mb/s based on the interleaving P/D transmission.

VI. IMPLEMENTATION AND SUMMARIZED RESULTS

The micrographs of the overall wireless microsystem are as shown in Fig. 12, including top-view, bottom-view and side-view of the microsystem, bending test, wireless P/D transmission, dissolvable μ-needles and die photo of die-2. The proposed wireless microsystem realizes 128-channel neural-signal sensing within the area of 5mm x 5mm, neural feature extraction and wireless P/D transmission. Table II presents the specifications and comparisons of the invasive neural-sensing microsystems with the planer structures. Accordingly, all parameters of this microsystem are notable.

VII. CONCLUSIONS

This paper presents a miniaturized implantable 128-channel wireless neural-sensing microsystem using TSV-embedded dissolvable μ-needle array, a flexible interposer and 4 dies by 2.5D/3D TSV heterogeneous SiP technology. The proposed wireless microsystem realizes 128-channel neural-signal sensing within the area of 5mm x 5mm, neural feature extraction and wireless power/data transmission using an on-interposer inductor. The overall average power of the circuits in this microsystem is only 9.85mW.

REFERENCES