Through-Silicon-Via-Based Double-Side Integrated System for Neural Sensing Applications

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Highly integrated and miniaturized neural sensing microsystems that provide stable observation, small form factor and biocompatible properties are crucial for brain function investigation and neural prostheses realization for capturing accurate signals from an untethered subject in his natural habitat [1, 2]. Such biomedical devices usually comprise sensors and CMOS circuits for biopotential acquisition, signal conditioning, processing and transmission. Many approaches have been reported, including stacked multichip [3, 4], microsystem with separated neural sensors [5] and monolithic packaged microsystem [6]. Regardless of the integration schemes, the collected weak signals from the sensor need to pass through a string of interconnections including wire bonding, flip-chip bonding and welding or soldering bonds to the processing circuits. The excessive interfaces and connections introduce noise and lead to bulky packaged systems.

This paper presents a Through-Silicon-Via (TSV) based double-side integrated microsystem for brain neural sensing applications. Figure 6.3.1 shows the structure of the double-side integrated microsystem. MEMS neural microprobe array and low-power CMOS readout circuit are fabricated on two sides of the same silicon substrate, and TSV’s are used to form a low impedance interconnection between the probe tips and the processing circuits. The excessive interfaces and connections introduce noise and lead to bulky packaged systems. This interface allows stacking of other CMOS chips onto the circuit side by TSV 3D IC technique.

Figure 6.3.2 summarizes the representative leakage characteristics and calibrated equivalent (parasitic) circuit model between two adjacent TSVs measured from the TSV test vehicle. The leakage current between two TSVs with 200μm pitch, is at the pA level. The TSV resistance and parasitic capacitance are 5.5mΩ and 34.2fF, respectively, with measurement frequency up to 10GHz.

The CMOS circuits are fabricated in a UMC 0.18μm process on 8-inch wafers. After the standard CMOS process, a front-side, via-last, solid-tube Cu TSV technology is applied to form TSVs with 200μm depth (height) and 30μm diameter. Next, a Redistribution Layer (RDL) is fabricated for the connections between TSV arrays and circuit input pads. Then, a deep etching process is applied on the back side of the wafer to form the microprobe array with Ion-Coupled Plasma (ICP) etching. Two more MEMS thin-film processes including 2μm-thick parylene-C deposition and 0.45μm-thick Pt/Ti lift-off are applied to form an isolation layer on silicon bulk and biopotential acquisition material, respectively. Finally, after chip dicing, the full device is encapsulated by 5μm-thick parylene-C as a passivation layer and the probe tips are exposed with Reactive Ion Etch (RIE) process. Only the platinum layer, which works as a sensing material, will directly contact the brain tissue.

The 16-channel low noise and low power read-out circuitry is designed using 16 two-stage Analog Front-End (AFE) circuits as shown in Figure 6.3.4. For each channel, the sensing signal is transmitted from the neural probes on the back side to the AFE circuit through the 3x8 TSV array as shown in Figure 6.3.1. The TSV array and the input of AFE circuit are connected by the Redistribution Layer (RDL) on the front-side of the silicon. The impedance of single TSV is only 5.5mΩ and 34.2fF, much smaller than traditional long transmission wires. Thus, the voltage drop and noise are reduced significantly compared with long transmission wires. The AFE is designed using a Differential Difference Amplifier (DDA) stage followed by a differential amplifier stage. The advantages of DDA are high input resistance, high CMRR and low noise. Moreover, the mismatch of resistors only influences the gain of DDA and would not affect its CMRR. To reduce flicker noise in low frequency neural signals, the input stage of the DDA is implemented using long-channel PMOSs (M0-M3) operated in the weak inversion region. M7-M15 realize the current mirror for converting the input voltage into current while transferring this to the output stages. The AB-class output stage (M18 and M19) is controlled by M16 and M17 based on the current, and Mc is the Miller capacitor to increase the phase margin. The design of the succeeding differential amplifier stage is similar to that of the preceding DDA stage with only one differential pair. The gain of the DDA stage and the differential amplifier stage are 20x and 25x, respectively. Each AFE circuit contains biasing circuitry to generate the biasing voltage (VP1, VP2 and VN1) for both stages.

Figure 6.3.5 presents the measurement results of the AFE circuitry. The voltage gain and bandwidth are 54.8dB and 7.3kHz, respectively. The low 3dB frequency is 0.41Hz to filter the DC offset and flicker noise. A CMRR of 168dB and PSRR of 72dB are achieved to suppress the common mode noise from human bodies and power supply noise. Total Harmonic Distortion (THD) and input-referred noise are -56dB and 1.08μVrms (0.1Hz to 5kHz), respectively. Figure 6.3.6 shows the specification of the microsystem. The total power of the 16-channel AFE circuitry is 351.2μW. Figure 6.3.7 shows the die micrograph, floorplan of the front-side and the layout view of the back-side.

References:
Figure 6.3.1: TSV-based double-side integrated microsystem.

Figure 6.3.2: TSV test vehicle and representative characterization results.

Figure 6.3.3: Measured impedance and SEM of fabricated MEMS microprobe array with TSV.

Figure 6.3.4: Schematic of single channel Analog Front-End (AFE) circuit.

Figure 6.3.5: Measurement results of the AFE circuitry.

Figure 6.3.6: Specification of the microsystem.